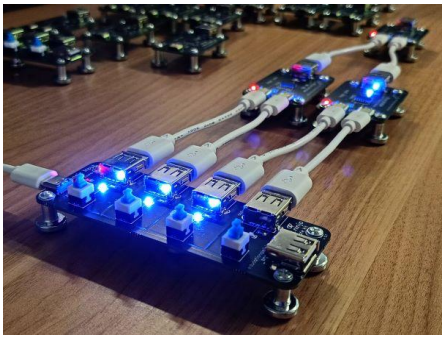
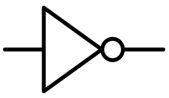
Logic Gates 001



1. Using the logic gates, complete the truth tables for the following

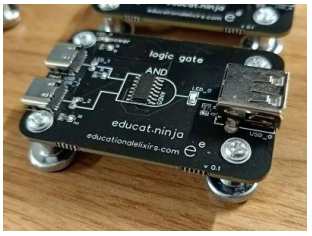
a. NOT



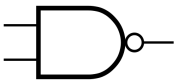
Input	Output
0	
1	

b. AND

Input A	Input B	Output
0	0	
0	1	
1	0	
1	1	



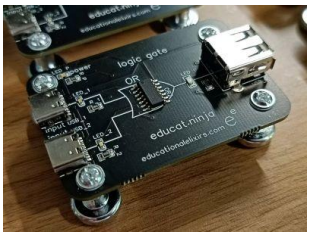
c. NAND



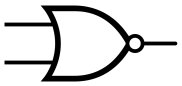
Input A	Input B	Output
0	0	
0	1	
1	0	
1	1	

d. OR

Input A	Input B	Output
0	0	
0	1	
1	0	
1	1	



e. NOR



Input A	Input B	Output
0	0	
0	1	
1	0	
1	1	

f. XOR

Input A	Input B	Output
0	0	
0	1	
1	0	
1	1	

2. Which alternative word might better describe an

    a. AND gate?

    b. OR gate?

3. Which single logic gate best matches the following sentences?

    a. “You can have a packet of crisps or a chocolate bar”

    b. “You will **go to prison** if you **murder someone** or **steal a car**”

    c. “Whatever you tell sophie to do, she will do the opposite”

    d. “You will make your tutor happy if you get an **A* in Chemistry** and an **A* in Computer Science**”

    e. “You may **go to university** if you don’t **get expelled** or **miss an exam**”

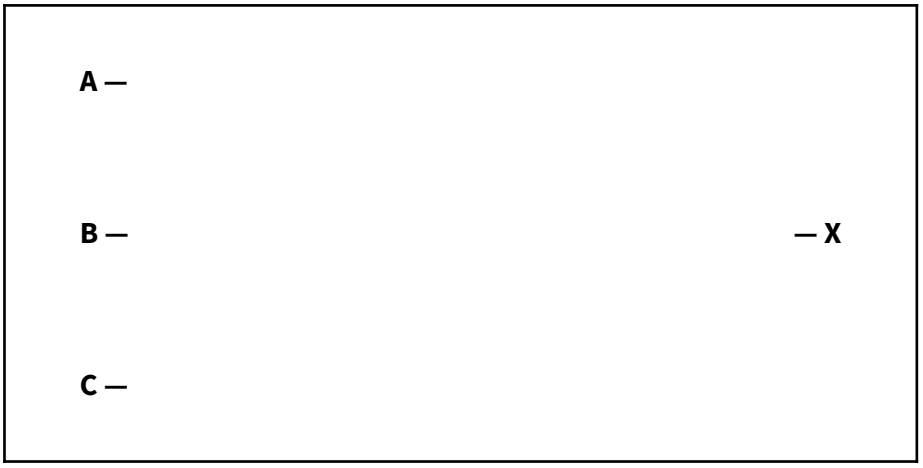
    f. “You will **live a long and happy life** if you don’t **eat unhealthy food** and **avoid exercise**”

Logic Gates `010`

1. Construct a simple logic gate circuit which could be used to switch a heater on only when the temperature is cold (OFF) and the doors are closed (ON).

2. Construct a simple logic circuit which will switch on only when input A is on, or when both inputs B and C are on. Draw the logic circuit below.

3. For the following logic statement, X = (((A XOR B) OR (NOT (B OR C))) AND C);
   a. draw a logic circuit to represent the given logic statement.

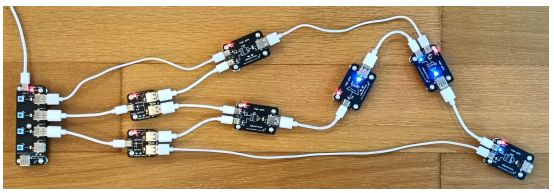


   b. Predict the truth table you would expect for the above circuit, use the blank columns for rough work if necessary.

A	B	C				X
0	0	0				
0	0	1				
0	1	0				
0	1	1				
1	0	0				
1	0	1				
1	1	0				
1	1	1				

   c. Construct the circuit and test (and correct if necessary) your answer

Your circuit should look similar to the one below.



Logic 011 - The half adder

Binary

“There are 10 types of people in the world, those who understand binary and those who don’t”

Binary represents numbers as a series of **1**s and **0**s. Base 10 , our usual counting system uses powers of ten to represent numbers.

10^3	10^2	10^1	10^0
1000s	100s	10s	1s
2	0	2	3
2 × 1000	0 × 100	2 × 10	3 × 1

2^3	2^2	2^1	2^0
8s	4s	2s	1s
1	0	1	1
1 × 8	0 × 4	1 × 2	1 × 1

2 000
0 00
2 0
3
2023

8
0
2
1
11

2023 in binary would be **11111100111** - 1024, 512, 256, 128, 64, 32, 0, 0, 4, 2, & 1.

As binary only has two states, it can be represented by ON and OFF, or TRUE and FALSE. It’s possible to use logic gates to add together numbers. We call each of these binary characters a ‘bit’. A byte is 8 bits, and can represent a number up to 255. Two bits can represent a number up to 3.

binary	base-10
00	0
01	1
10	2
11	3

Binary addition

There are 4 possible combinations of two bits

	binary	base-10	binary	base-10	binary	base-10	binary	base-10
A	0	0	0	0	1	1	1	1
B	+ 0	+ 0	+ 1	+ 1	+ 0	+ 0	+ 1	+ 1
	00	0	01	1	01	1	10	2

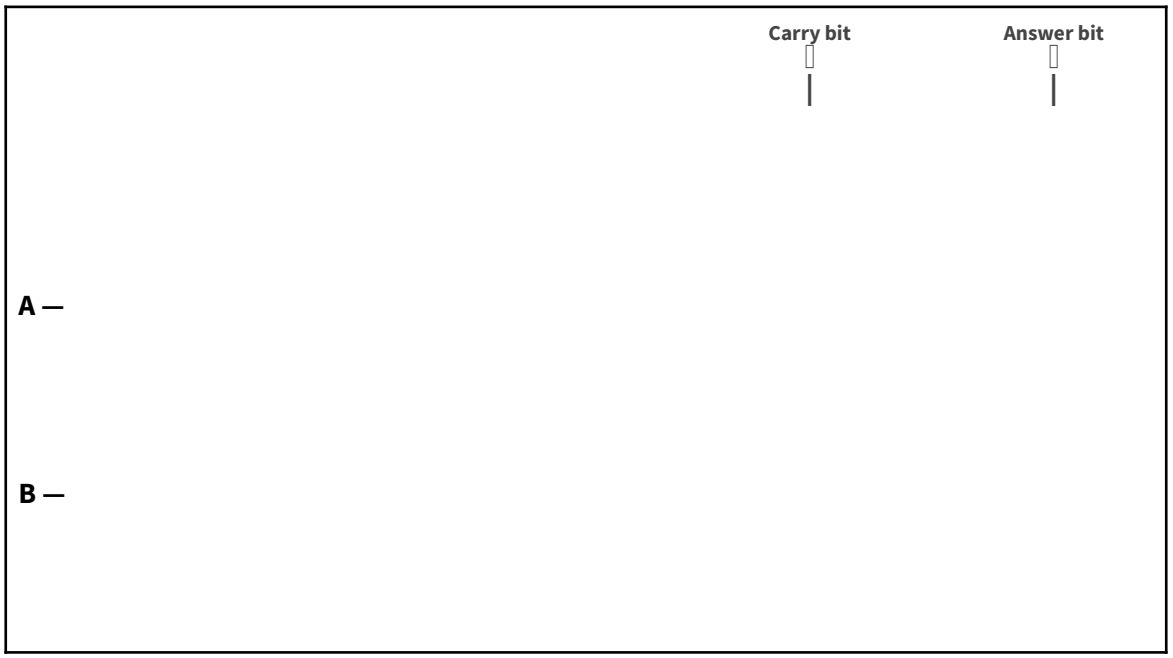
We can use logic gates to combine the inputs which will add together the two numbers to make a 1-bit adder. As the answer could be 2, we need two output bits to represent it. The underlined bit is usually referred to as the **sum** bit and the other bit is the **carry** bit.

Using the highlighted input, construct a truth table for the two output bits.

Input A	Input B	Output (carry)	Output (sum)
0	0		
0	1		
1	0		
1	1		

Which logic gates could be used to produce the same output?

Draw a logic circuit to combine the two inputs to give two outputs for the two binary digits.



Construct the logic circuit using the Logic Gate Kit to test it. Correct your logic circuit above if necessary. You have just made a **half adder**.

The carry bit

When you add 37 to 28, you can start by adding 7 to 8 and getting 15. The 5 is the answer digit and the 1 (10) is the carry digit. The carry digit is then combined with the 3 (from the **3**7) and the 2 (from the **2**8), to give 6 (60).

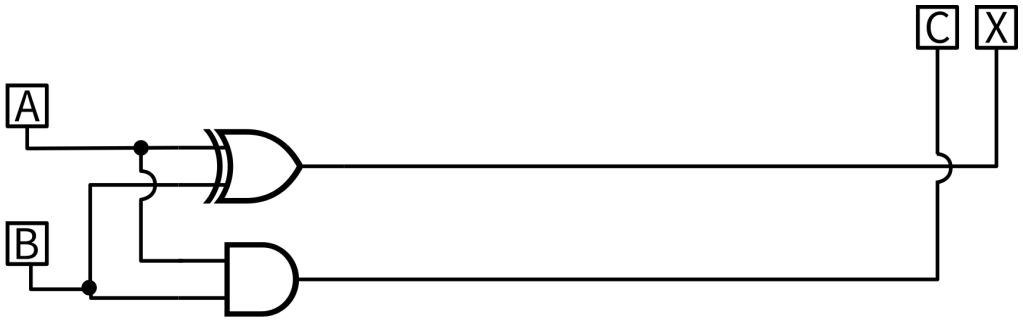
$$\begin{array}{r} 3\,7 \\ +\,2\,8 \\ \hline 6\,\mathbf{5} \end{array}$$

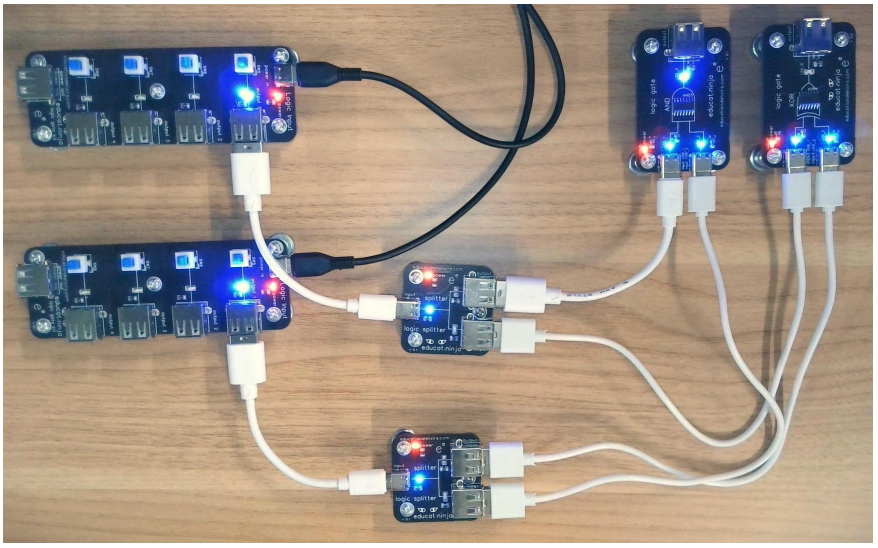
$3 + 2 + \underline{1}$	$7 + 8$
$= 6$	$= \underline{1}\mathbf{5}$
$\underline{1}$	☒ Carry ‘bit’

If you want to add multi-bit binary numbers together you need to combine 3 inputs, the two digit inputs and also the carry bit.

Logic 100 - The full adder

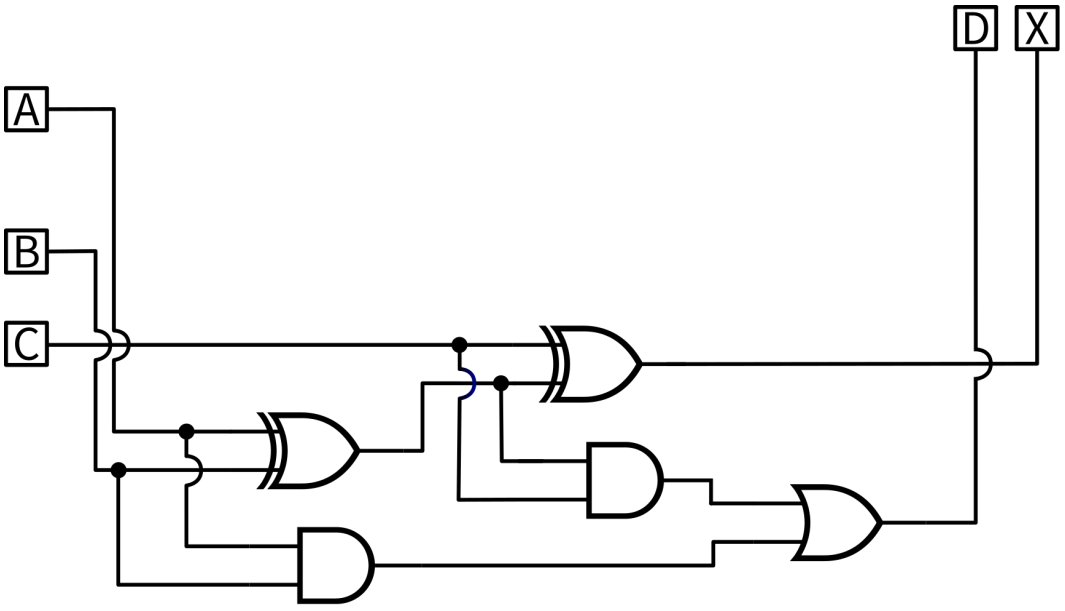
The logic circuit for a half adder is shown below to combine one-bit binary numbers together. The output is a two-bit number, a sum bit, **X** and the carry bit **C**.





A working half adder constructed from the educat.ninja modular logic gate kit

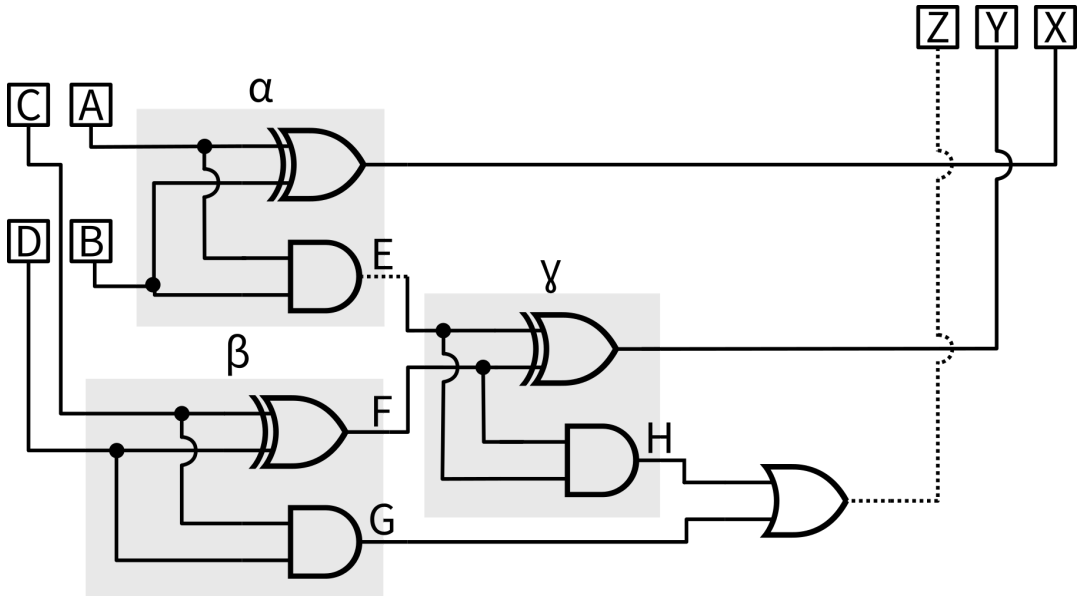
The logic circuit for a full adder is shown below. **C** is the carry bit input from a preceding adder.



Q. Draw, and then build, the logic circuit combining the half and full adder to allow addition of two 2-bit binary numbers. There will be 3 output bits, two sum bits and a carry bit. You will need an input board (ideally two input boards to represent the two numbers being added together), three XOR, two AND, and an OR gate, together with 6 splitters.

Logic Gates 101 - Review - The full and half adder combined, 2-bit addition

Using logic gates two two-bit numbers, CA and DB, can be added together. Below is a combination of a half and a full adder. The carry bits are highlighted by the dotted lines.

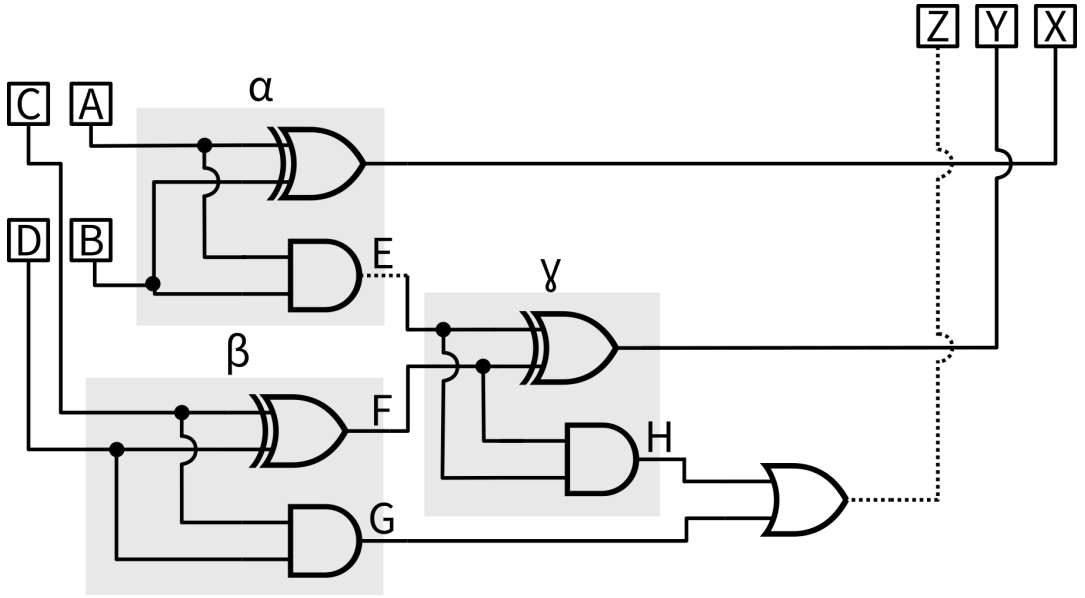


Q. Complete the truth table for the above logic circuit then build to check your answers.

INPUT								**OUTPUT**		
				A AND B			E AND F			A XOR B
C	**A**	**D**	**B**	**E**	**F**	**G**	**H**	**Z**	**Y**	**X**
0	0	0	0							
0	0	0	1							
0	0	1	0							
0	0	1	1							
0	1	0	0							
0	1	0	1							
0	1	1	0							
0	1	1	1							
1	0	0	0							
1	0	0	1							
1	0	1	0							
1	0	1	1							
1	1	0	0							
1	1	0	1							
1	1	1	0							
1	1	1	1							

A closer look again at a two-bit adding circuit.

The circuit is composed of three half-adders. A single half-adder (**α**) operating on the smallest bits, **A** and **B**. The 'second' bits are first combined in half-adder (**β**), before the output is combined with the carry bit from **α** in the third half-adder (**γ**). These two half adders when combined together and with an OR gate (for the carry bit) is called a **full adder**.



A full adder adds together 3 input bits, **C**, **D** and **E**, the carry bit from a previous adder. The first bits (**A** & **B**) can be combined with only a half adder as there is no input carry bit.

Below are a selection of additions and their expected results.

00	00	01	10	00	11	11
+ 00	+ 01	+ 00	+ 00	+ 10	+ 10	+ 11
000	001	001	010	010	101	110

Convert the following numbers from binary to base-10 or base-10 to binary as appropriate.

1. 0101
2. 1101
3. 0011
4. 1010
5. 1111

6. 7
7. 2
8. 11
9. 14
10. 4

Logic Gates 110 - Universal Challenge

1. Using **only NAND gates** (and splitters where necessary), start by writing the truth table and then construct and draw the logic circuit diagram for
    a. a NOT gate (requires only one NAND gate)

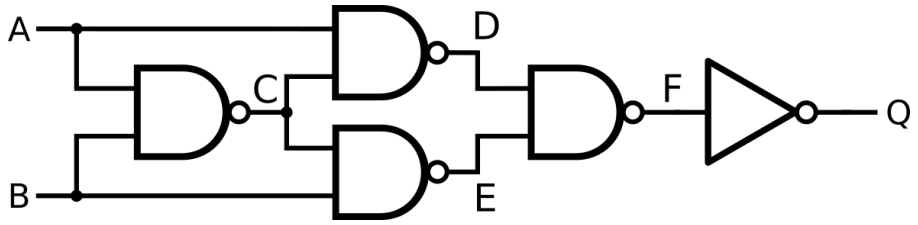
    b. an AND gate (requires 2 NAND gates)

    c. an OR gate (requires 3 NAND gates)
    Hint: Start by drawing the truth tables for the OR and NAND gates - can you see a way to flip the truth table outputs upside down? This gate can also be achieved with two NOT gates and a NAND gate).

    d. a NOR gate (requires 4 NAND gates)

    e. an XOR gate (requires 4 NAND gates)

2. The XNOR gate can be generated from 4 NAND gates and a NOT gate as shown below



a. Another name for the XNOR gate is NXOR. Based on the difference between the truth tables for the AND/NAND and OR/NOR gates, predict the expected truth table for the XNOR gate.

A	B	Q
0	0	
0	1	
1	0	
1	1	

b. Complete the truth table below for the above logic circuit.

A	B	C	D	E	F	Q
0	0					
0	1					
1	0					
1	1					

c. Build the above logic circuit and check your answer - correct it if necessary. Demonstrate your completed logic circuit to your teacher.

d. Does this gate produce the expected truth table for the “NXOR” Gate?

3. “*The AND gate is an inverted input NOR gate*”.

Explain this statement as fully as possible with the use of a circuit diagram and a (long) truth table (similar to Q 2b).

4. Using only NOR gates, construct, and then draw, the logic circuit diagram for
    a. a NOT gate (requires a single NOR gate)

    b. an OR gate (requires 2 NOR gates)

    c. an AND gate (requires 3 NOR gates)

    d. a NAND gate (requires 4 NOR gates)

Challenging

    e. an XOR gate (requires 4 NOR gates ***and*** a NOT gate)